UNITRODE

APPLICATION NOTES

NEW DRIVER ICs OPTIMIZE HIGH SPEED POWER MOSFET SWITCHING CHARACTERISTICS

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ABSTRACT

Although touted as a high impedance, voltage controlled device, prospective users of Power MOSFETs soon learn that it takes high drive currents to achieve high speed switching. This paper describes the construction techniques which lead to the parasitic effects which normally limit FETperformance, and discusses several approaches useful to improve switching speed. A series of drivers ICs, the UC3705, UC3706, UC3707 and UC3709 are featured and their performance is highlighted. This publication supercedes Unitrode Application Note U-98, originally written by R. Patel and R. Mammano of Unitrode Corporation.

INTRODUCTION

An investigation of Power MOSFET construction techniques will identify several parasitic elements which make the highly-touted "simple gate drive" of MOSFET devices less than obvious. These parasitic elements, primarily capacitive in nature, can require high peak drive currents with fast rise times coupled with care that excessive di/dt does not cause current overshoot or ringing with rectifier recovery current spikes.

This paper develops a switching model for Power MOSFET devices and relates the individual parameters to construction techniques. From this model, ideal drive characteristics are defined and practical IC implementations are discussed. Specific applications to switch-mode power systems involving both direct and transformer coupled drive are described and evaluated.

POWER MOSFET CHARACTERISTICS

The advantages which power MOSFETs have over their bipolar competitors have given them an ever-increasing utilization in power systems and, in the process opened the way to new performance levels and new topologies.

A major factor in this regard is the potential for extemely fast switching. Not only is there no storage time inherent with MOSFETs, but the switching times can be user controlled to suit the application. This or course, requires that the designer have an understanding of the switching dynamics inherent in these devices. Even though power MOSFETs are majority carrier devices, the speed at which they can switch is dependent upon many parameters and parasitic effects related to the device's construction.

THE POWER MOSFET MODEL

An understanding of the parasitic elements in a power MOSFET can be gained by comparing the construction details of a MOSFET with its electrical model as shown in Figure 1. This construction diagram is a simplified sketch of a single cell - a high power device such as the IRF 150 would have ≈ 20,000 of these cells all connected in parallel.

In operation. when the gate voltage is below the gate threshold, Vg(th), the drain voltage is supported by the N-drain region and its adjacent implanted P region and there is no conduction.

When the gate voltage rises above Vg(th), however, the P area under the gate inverts to N forming a conductive layer between the N+ source and the N-drain. This allows electrons to migrate from source to drain where the electric field in the drain sweeps them to the drain terminal at the bottom of the structure.

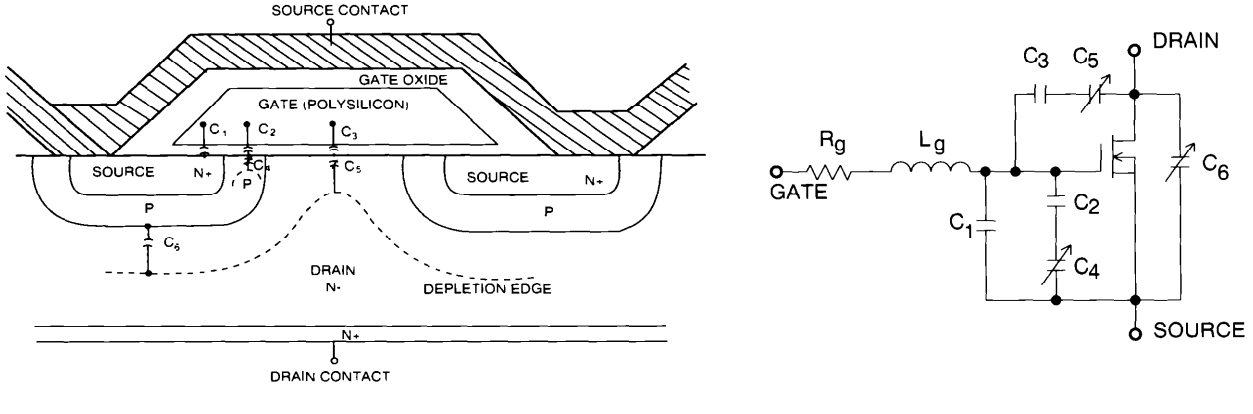


FIGURE 1 - SIMPLIFIED CROSS SECTION OF A POWER MOSFET CELL AND ITS ELECTRICAL EQUIVALENT.

In the equivalent model. the parameters are defined as follows:

1. Lg and Rg represent the inductance and resistance of the wire bonds between the package terminal and the actual gate, plus the resistance of the polysilicon gate runs.

2. C1 represents the capacitance from the gate to both the N+ source and the overlying source interconnecting metal. Its value is fixed by the design of the structure.

3. C2 + C4 represents additional gate-source capacitance into the P region. C2 is dielectric capacitance and is fixed while C4 is due to the depletion region between source and drain and varies with the gate voltage. Its contribution causes total gate-source capacitance to increase 10-15% as the gate voltage goes from zero to Vg(th).

4. C3 + C5 is also made up of a fixed dielectric capacitance plus a value which becomes significant when the drain to gate voltage potential reverses polarity.

5. C6 is the drain-source capacitance and while it also varies with drain voltage, it is not a significant factor with respect to switching times.

EVALUATING FET PARASITIC ELEMENTS

Although it is clearly not the best way to drive a power MOSFET, using a constant gate current to turn the device on allows visualization of the capacitive effects as they affect the voltage waveforms. Thus the demonstration circuit of Figure 2 is configured to show the gate dynamics in a typical buck-type switching regulator circuit. This simulates the inducitve switching of a large class of applications and is implemented here with a IRF-510 FET, which is a 4 amp, 100V device with the following capacitances:

Ciss ≈ C1 + C4 + C5 = 135 - 150 pF

Crss ≈ C5 = 20 - 25 pF Vgs = 0V

Coss ≈ C5 + C6 = 80-100 pF

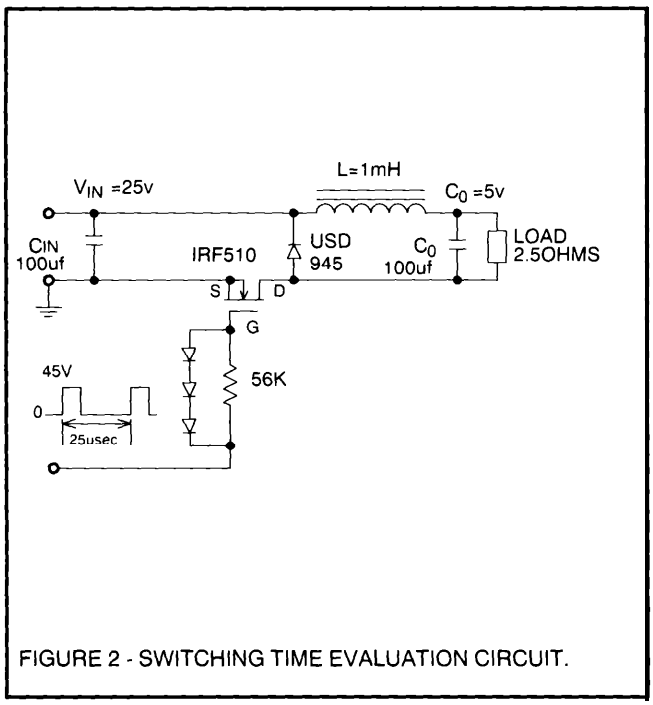


FIGURE 2 - SWITCHING TIME EVALUATION CIRCUIT.

In this illustration the load portion of the circuit is established with Vin = 25V. Io = 2A. and f = 25Khz. The resultant turn-on waveforms are shown in Figure 3 from which the following observations may be made:

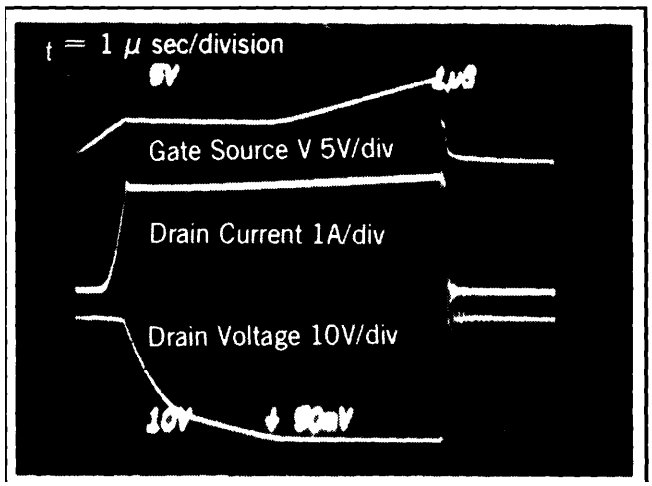


FIGURE 3-FET TURN-ON SWITCHING CHARACTERISTICS WHEN DRIVEN WITH A CONSTANT GATE CURRENT

1. For a fixed gate drive current, the drain current rise time is 5 times faster than the voltage fall time.

2. There is a 10-15% increase in gate capacitance when the gate voltage reaches Vg(th).

3. The gate voltage remains unchanged during the entire time the drain voltage is falling because the Miller effect increases the effective gate capacitance.

4. The input gate capacitance is approximately twice as high when drain current is flowing as when it is off.

5. The drain voltage fall time has two slopes because the effective drain-gate capacitance takes a significant jump when the drain-gate potential reverses polarity.

6. Unless limited circuit inductance, the current rise time depends upon the large signal g_M and the rate of change of gate voltage as $\Delta Id = g_M \Delta Vg$

CHANGES IN EFFECTIVE CAPACITANCE

The waveform drawings of Figure 4 illustrate the dynamic effects which take place during turn-on. As the gate voltage rises from zero to threshold. C2 is not significant since C4 is very small. At threshold, the drain current rises quickly while the drain voltage is unchanged. This, of course, is due to the buck regulator circuit configuration which will not let the voltage fall until all the inductor current is transferred from the free-wheeling diode to the FET.

While the drain current is increasing, there is a slight increase in the gate capacitance due to the large current density underneath the gate in the N-region close to the P areas.

As the drain voltage begins to fall, its slope depends upon gate to drain capacitance and not that from gate to source. During this time, all the gate current is utilized to charge this gate to drain capacitance and no change in gate voltage is observed. This capacitance initially increases slightly as the voltage across it drops but then there is a significant jump in value when the drain falls lower than the gate. When the polarity reverses from drain to gate, a surface charge accumulation takes place and the entire gate structure becomes part of the gate to drain capacitance. At this point the drain voltage fall time slows for the duration of its transition.

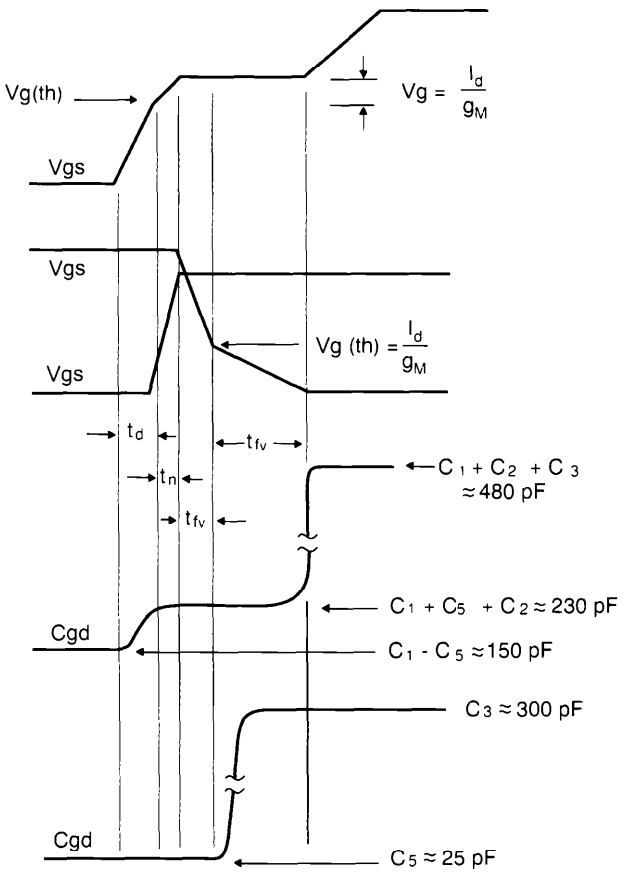


FIGURE 4 - Parasitic CAPACITANCE VARIATION FOR A UFN510 MOS FET DURING TURN-ON

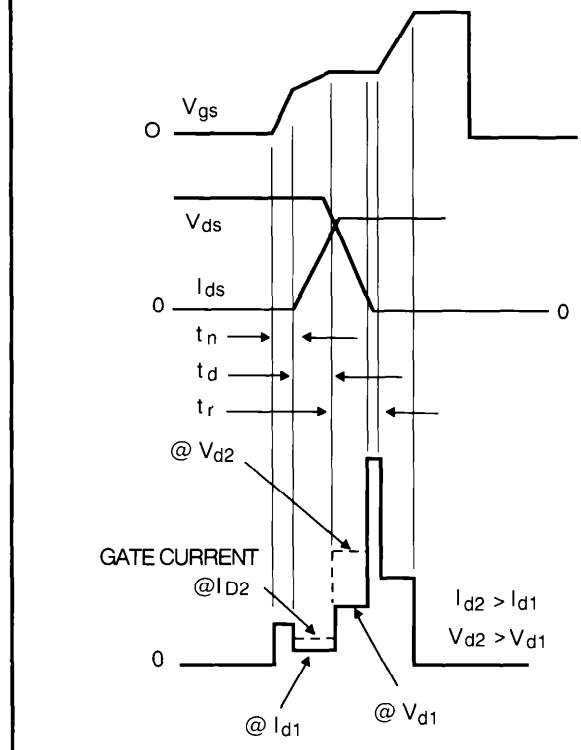


FIGURE 5 - AN "IDEAL" GATE CURRENT TURN-ON DRIVE TO PROVIDE EQUAL CURRENT RISE AND VOLTAGE FALL TIMES WITH AN INDUCTIVE LOAD

AN OPTIMUM GATE DRIVE

In most switching power supply applications, if a step function in gate current is provided, the drain current rise time is several times faster than the voltage fall time. This can result in substantial switching power losses which are most often combated by increasing the gate drive current. This creates a problem, however, in that it further reduces current rise time which can cause overshoot, ringing, EMI and power dissipation due to recovery time for the rectifiers which are much happier with a more slowly changing drain current.

In an effort to meet these conflicting requirements, an idealized gate current waveform was derived based upon the goal of making the voltage fall time equal to the current rise time. This optimum gate current waveform is shown in Figure 5 and consists of the following elements

1. An initial fast pulse to get the gate voltage up to threshold.

2. A lesser amount to slow the drain current rise time. This value however, will also be a function of the required drain current.

3. Another increase to get the drain voltage to fall rapidly with a large current pulse added when the drain gate potential reverses.

4. A continued amount to allow the gate voltage to charge to its final value.

Obviously this might be a little difficult to implement in exact form, however, it can be approxtimated by a gate current waveform which, instead of being constant, has a rise time equal to the desired sum of the drain current rise time and the voltage fall time, and a peak value high enough to charge the large effective capacitance which appears during the switching transition. The peak current requirement can be calculated on the basis of defining the amount of charge required by the parasitic capacitance through the switching period.

A linear current ramp will deliver a charge equal to

$$Q = \frac{Ip \cdot ton}{2} \qquad \text{where we define } ton = td + tn + tfv$$

The total charge required for switching is

$$Q = Ciss\,[Vg(th) - \frac{Id}{g_M}] - Crss\,[V_{DD} - Vg(th)] - Crss\,V_g(th)$$

where Crss' is the gate-drain capacitance after the polarity has reversed during turn-on and is related to Ciss by the basic geometry design of the device. A reasonable approximation is that Crss'≈1.5 Ciss. With this assumption.

$$Ip \approx \frac{2}{ton}\left[Ciss\left(2.5Vg(th) + \frac{Id}{g_M}\right) + Crss\left(V_{DD} - Vg(th)\right)\right]$$

As an example, if one were to implement a 40V. 10A buck regulator with a UFN150, it would not be unreasonable to extend the total switching time to 50 nsec to accomodate rectifier recovery time. An optimum drive current for this application would then take 50 nsec to ramp from zero to peak value calculated from

Ciss = 2000pF *ton = 50nsec*
Crss = 350pF v_{DD} = 40*V*
Vg(th)=3V *Id*= 10A

$$g_M = \frac{10A}{2.5V} = 4s$$

$$\text{as } Ip = \frac{2}{50 \times 10^{-9}}\left[2000 \times 10^{-12}\left(2.5 \times 3 + \frac{10}{4}\right) + 350 \times 10^{-12}(40 - 3)\right]$$

$\therefore$ *Ip = 1.32 amps peak*

The above has shown that while high peak currents are necessary for fast power MOSFET switching, controlling the rise time of the gate current will yield a more well-behaved system with less stress caused by rectifier recovery times and capacitance. This type of switching requirement can be fulfilled with integrated circuit technology and several IC's have been developed and applied as MOSFET drivers.

TOTAL GATE CHARGE (Qg)

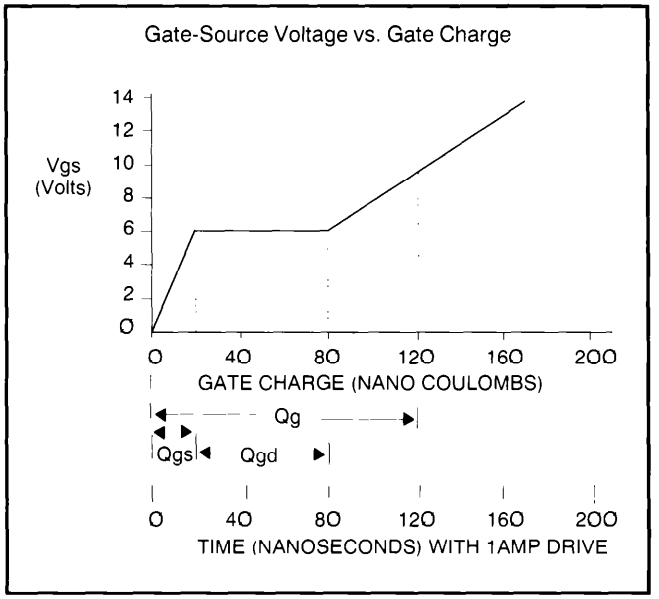
Another approach used to quantify and understand MOSFET gate drive requirements is much simpler than that of examining the instantaneous voltages, currents and capacitances. The term "Total Gate Charge", or Qg specifies the amount of gate charge required to drive the FET gate-to-source voltage (Vgs) from zero to ten volts, or vice-versa. For most high voltage devices these thresholds correspond to the FET being either completely on or off.

Charge (Q) can be expressed as the product of either current multiplied by time (I*T), or capacitance multiplied by voltage (C*V) in the units of Coulombs. Most contemporary devices have total gate charge requirements in the tens to low hundreds of nano Coulombs dependent almost entirely on die's geometry. For example, an IRF710 (size 1) FET has a total gate charge requirement of only 7.7 nC whereas the IRFP460 (size 6) demands 120 nC, and both are typical values.

PARAMETER	IRFP 440	IRFP 450	IRFP 460
Qgs (NC)	6.2	11	18
Qgd (NC)	22	43	62
Qg (NC)	42	86	120
Ciss (Nf)	1.3	2.7	4.1

There are two specified parameters contained within the total gate charge expression: Qgs, the gate-to-source charge, and Qgd the gate-to-drain, or "Miller" charge. Qgs is the amount of charge required to bring the gate voltage from zero up to its threshold VGS (th), of approximately 6 volts. Qgd defines the amount of charge that must be input to overcome the "Miller" effect as the drain voltage falls. This occurs during the plateau of the gate-to-source voltage waveform where the voltage is "constant". Excess charge is added to lower the effecive Rds (on) until the gate voltage reaches 10 volts wher Qg is specified. Further increases above this level do NOT lower Rds (on), so a 10-12 volt driver bias is ideal.

The total charge curve can be examined in sections to define the ideal driver's characteristics. Using a constant current of 1 ampere, the total charge curve (Qg=I*T) in nanoCoulombs also represents the MOSFET turn-on delay, drain current rise and drain voltage fall times in nanoseconds.



First of all, and most importantly, the average capacitive load represented by the FET to the IC driver is NOT the specified MOSFET input capacitance, Ciss. The effecive input capacitance, Ceff, is the total charge divided by the final gate voltage, Vgs(f);

Ceff = Qg(total) / Vgs(f).

Using the total gate charge curve show above, the 460 FET with Vds (off) = 400 volts has an effective input capacitance (Ceff) of approximately 120nC/10v, or 12 nF during the interval of 0 < Vgs < 10v. The specified input capacitance of Ciss = 4.1 nF applies only at Vgs=O, and is often mistaken for the driver's actual load.

The Qgs portion of the curve is primarily governed by the driver's ability to quickly turn ON. Therefore, a sharp, fast transition of the totem-pole output from low to high is essential to minimize the delays from 0 < Vgs < VGS (th). In most applications the driver IC is not peak current limited during this interval, since it is more likely to be dV/dT limited. The effective gate (load) capacitance is approximately Qgs/VGS(th). or Ciss.

Evident from the charge specifications, most of the popular size FETs used in switch-mode power supplies (sizes 4. 5 and 6) have much larger Qgd demands than their gate-to-source counterpart, Qgs. During this Qgd interval, the gate voltage remains "constant" while gate charge accumulates and the drain voltage collapses. It is also during this period that most drive circuits are simply peak current limit, whether by the driver IC or an external resistor. High peak currents are necessary for fast transitions through this interval, especially when driving large geometry FETs.

Full drain current is flowing at the beginning of the Qgd portion of the Qg curve, and notice that the drain voltage remains high. FET power loss is at its maximum here, and decreases linearly with Vds. A majority of the Qgd charge goes to combat the "Miller" effects as the drain voltage falls from that of its off condition to Vgs, or approximately Vgs(th). The remainder of the charge is used to bring the drain voltage down below that of the gate. decreasing the

effecive gate capacitance over the Qgd interval since there is relatively no change in gate voltage. The important fact, however, is that high peak currents are needed to minimize the FET power loss and transition time.

The remainder of the gate charge brings the gate voltage from VGS (th) to 10 volts. This "excess" charge reduces the FET "ON" resistance to its minimum, and raising the gate voltage above 10 volts has no further effect on reducing the Rds (on). The effective gate capacitance, which is high, can be obtained by dividing the charge input by the change in gate voltage during this region.

Ceff = [Qg - (Qgd+Qgd)] / (10v - VGS (th)) = 40nC/4v = 10nF for the IRFP460

FET DRIVER ICS

In searching for IC's capable of providing the fast transitions and high peak currents required by power MOSFETs. one of the first devices which became popular was the DS0026. While this IC was originally designed to be dual clock driver for MOS logic it was capable of supplying up to 1.5 amps as either a source or sink. In addition, it was made with a gold doped, all NPN process which minimizes storage delays, and as a result, offers transition times of approximately 20 nsec. Its disadvantages, however, are high cross conduction currents, as well as requiring excessive supply current when the output is in the low (OFF) state. This leads to higher power dissipation and junction temperature than optimum.

This brings us to newer ICs designed specifically as power MOSFET drivers for switchmode power supply applications. Several factors were taken into consideration while developing the new UC3705 /06 /07 /09 series of high current drivers: the most important of which, was to isolate the high power switching noise from the low level analog signals at the PWM. Seperate supply and return paths at the driver to its signal inputs and power outputs further enhances noise immunity. Additionally, several desirable features including an analog shutdown comparator have been incorporated in the UC3706 and UC3707 devices, whereas the UC3705 and UC3709 drivers are optimized for low cost applications which incorporate this function elsewhere in the design. Each driver features TTL compatible input thresholds, undervoltage lockout, thermal shutdown and low cross-conduction, high speed output circuitry. The corresponding block diagrams and pin assignments are shown in figures 6 thru 9, and followed by the feature selection index.

UC3705 Block Diagram

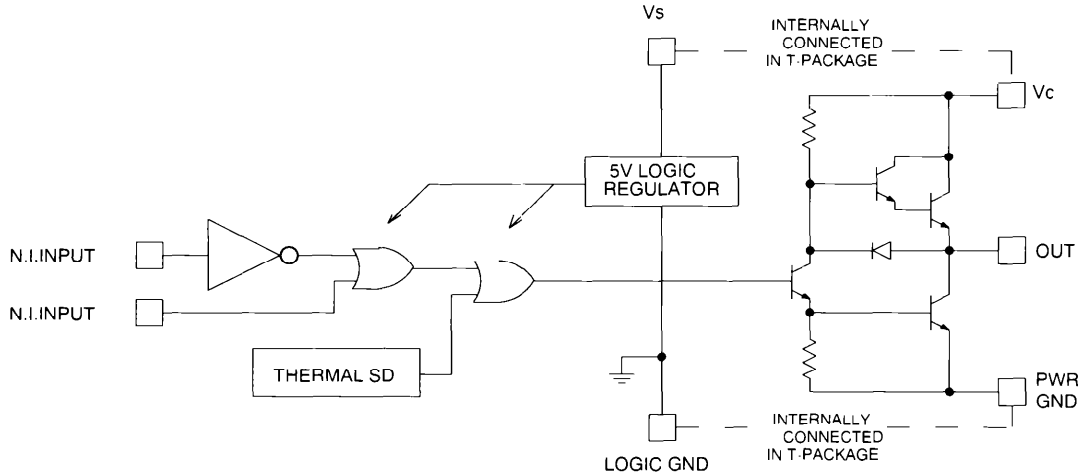


Figure 6

UC3706 Block Diagram

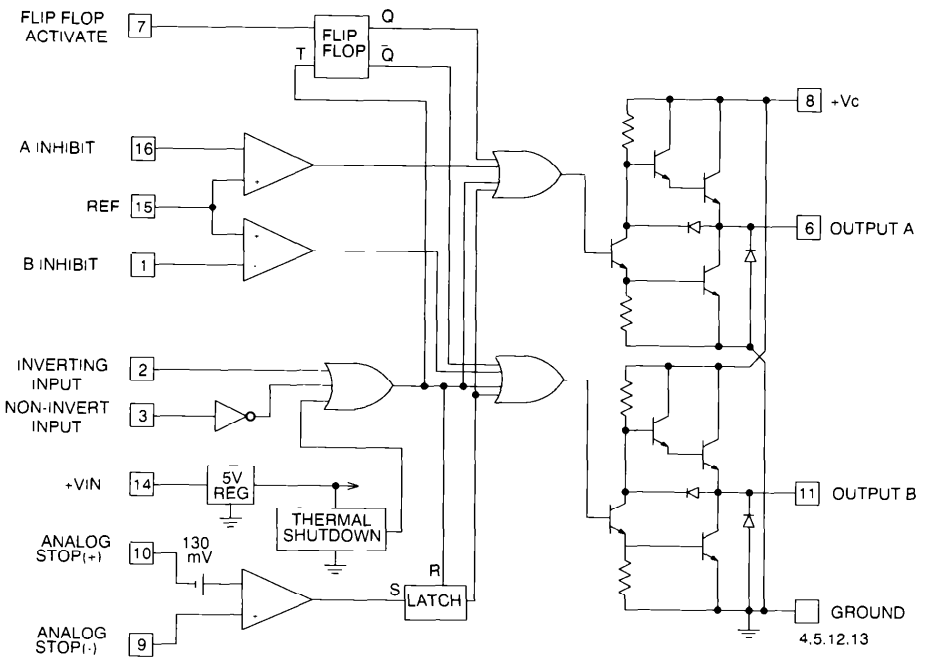


Figure 7

UC3707 Block Diagram

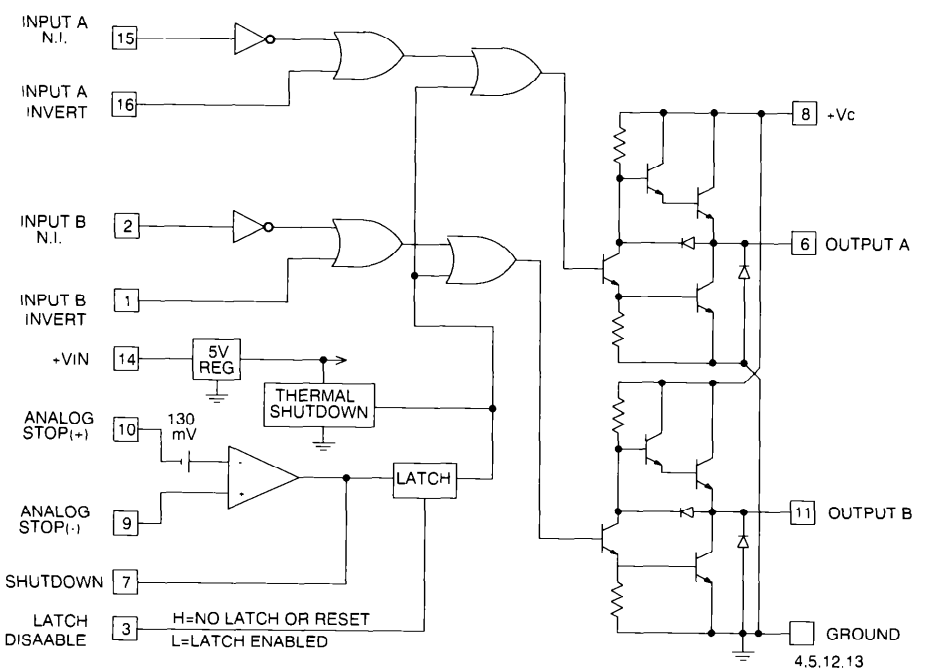
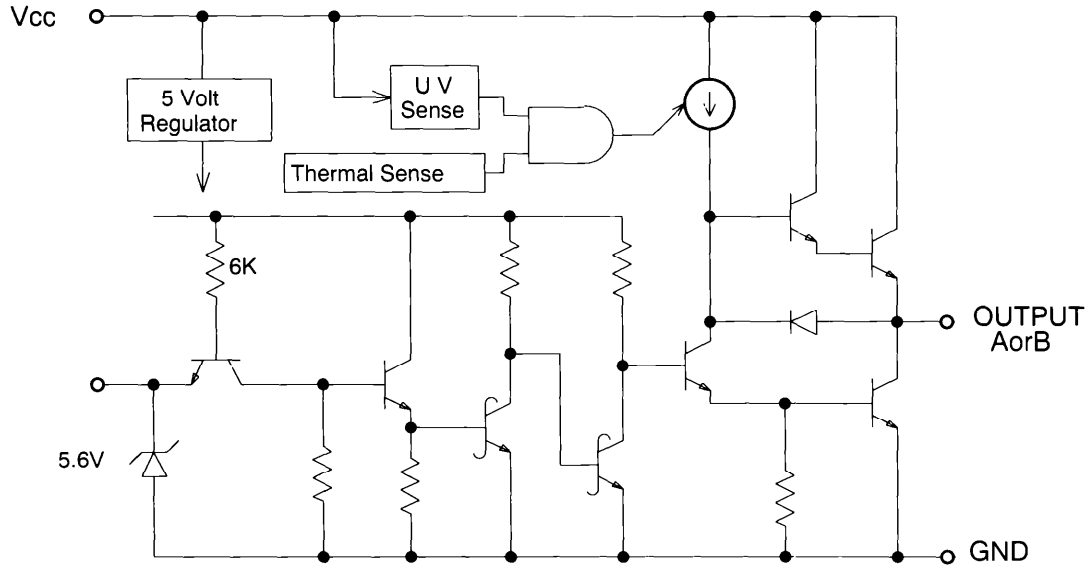


Figure 8

UC3709 Block Diagram



NOTE: One Output Shown

Figure 9

DRIVER FEATURES

1.5 Amp Peak Output Current (Per Output)

- 40 Nanosecond Rise & Fall Times into 1 NF
- Low Cross Conduction Current Spike
- 5 to 40 Volt Operation
- High Speed Power MOSFET Compatable
- Thermal Shutdown Protection

	DUAL OUTPUTS	INVERTING INPUTS	NON-INVERTING INPUTS	SEPERATE V_C & V_{IN}	SEPERATE PGND & SGND	ANALOG SHUTDOWN	DIGITAL INHIBIT	TOGGLE F/F	LATCH RESET
UC3705		X	X	X	X				
UC3706	X	X	X	X	X	X	X	X	
UC3707	X	X	X	X	X	X	X		X
UC3709	X	X							

1.5 AMP PEAK TOTEM-POLE OUTPUTS

The schematic of the UC3706 output drive circuit is shown in figure 10, which is similar to the other devices in this family. While first appearing as a fairly conventional totem-pole design, the subtleties of this circuit are the slowing of the turn-off of Q3 and the addition of Q4 for rapid turn-off of Q8. The result is shown in figure 11 where it can be seen that while maintaining fast transition times the cross conduction current spike has been reduced to zero when going low and only 20 nsec with a high transition. This offers negligible increase in internal circuit power dissipation at frequencies in excess of 500KHz.

Typical Output Schematic

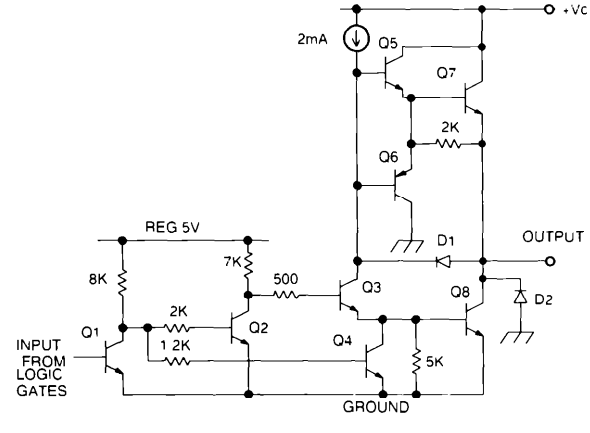


Figure 10

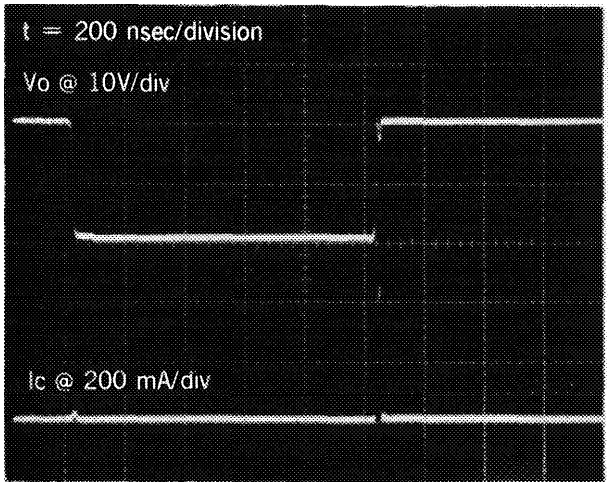


Figure 11

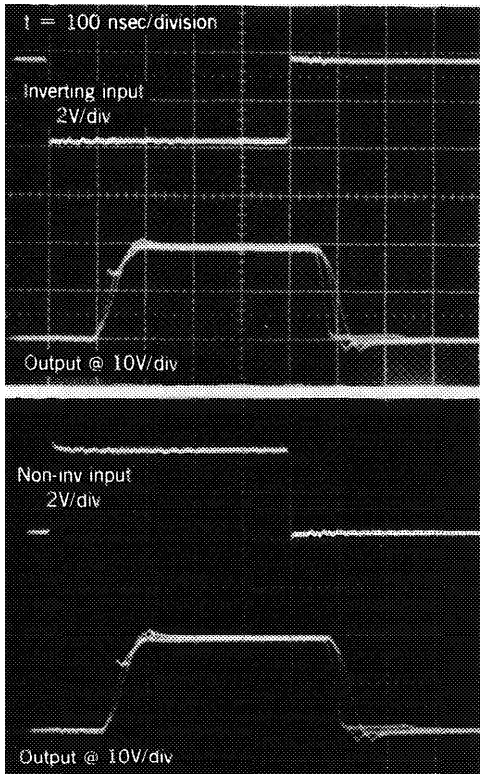


Figure 12

The overall transition time through the UC3706 is shown in figure 12 with the upper photograph recording the results with a drive to the inverting input while the lower picture is with the non-inverting input driven. Note that the only difference in speed between the two inputs is an additional 20 nSec delay in turning off when the non-inverting input is used. Here, and in further discussions note that ON and OFF relate to the driven output switch, i.e., On is with the output HIGH, and vice versa. The shutdown, inhibit and protective functions all force the output LOW when active.

Note that the typical rise and fall times of the output waveform average 20 nsec with no load, 25 nsec with 1 nF, and 35 nsec when the capacitive load is 2.2 nF at room temperature. Multilayer ceramic capacitors are used in this test and located as physically close to the IC output as possible to minimize lead and connection inductance.

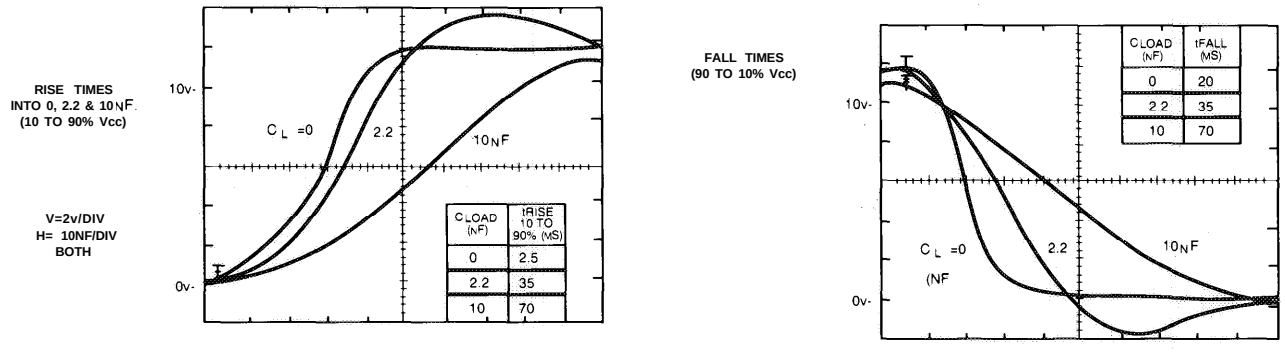


Figure 13

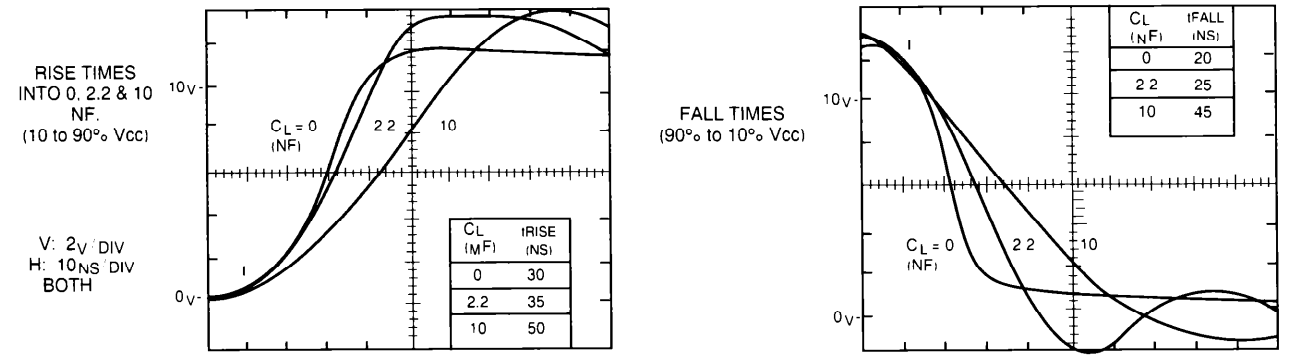


Figure 14

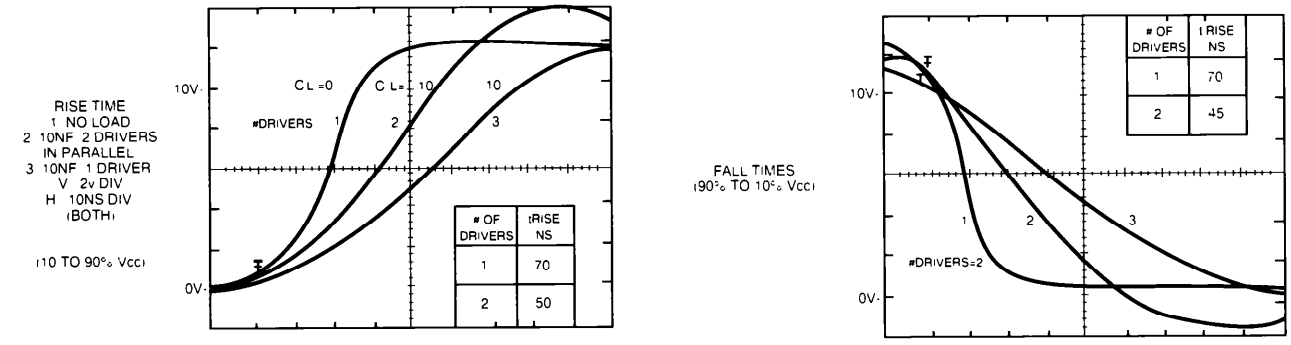


Figure 15

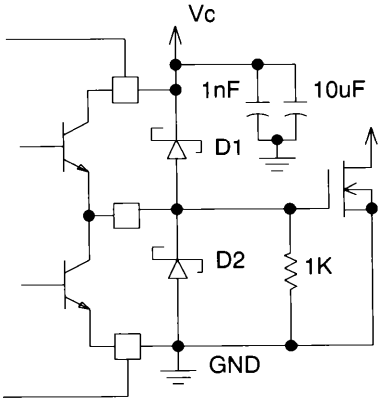
The peak current of each totem-pole output, whether source or sink, is 1.5 amps. However, on dual output versions like the UC3706, UC3707 and UC3709, both of the outputs can be paralled for 3 amp peak currents. In close proximity on the same die, each output virtually shares identical electrical and thermal characteristics. Saturation voltage is high at this current level but falls to under 2V at 500ma per output. Examples of typical switching characteristics are displayed.

It should be noted that while optimized for driving power MOSFET device, the UC3705 /06 /07 /09 ICs perform equally well into bipolar NPN transistors. In a steady-state off condition, the output saturation voltage is less than 0.4 volts as currents to 50 milliamps.

DIRECT COUPLED MOSFET DRIVE

The circuit of figure 17 shows the simplest interface to a power mosfet, direct coupling. In this example, an IRFP460 will be used to demonstrate the typical rise and fall times obtainable with a single 1.5 amp peak totem-pole driver. Further testing will include paralleling both outpus of a dual driver for a 3 amp peak capability. The IRFP460 device was selected, being the largest commercially

POWER MOSFET DRIVE CIRCUIT



D1 .D2:UC3611 SCHOTTKY DIODES

Figure 16

available FET die (a size “6”) at the time of this writing whose specifications were listed previously.

The typical values of each charge will later be used in conjunction with the measured driver performance to estimate the actual peak current delivered during each interval of turn-on. The tests shown were conducted at room temperature with the FET located directly at the IC output pins to nullify any effects of series inductance. Additional tests and measurements will demonstrate the effects of circuit inductance on gate driver performance.

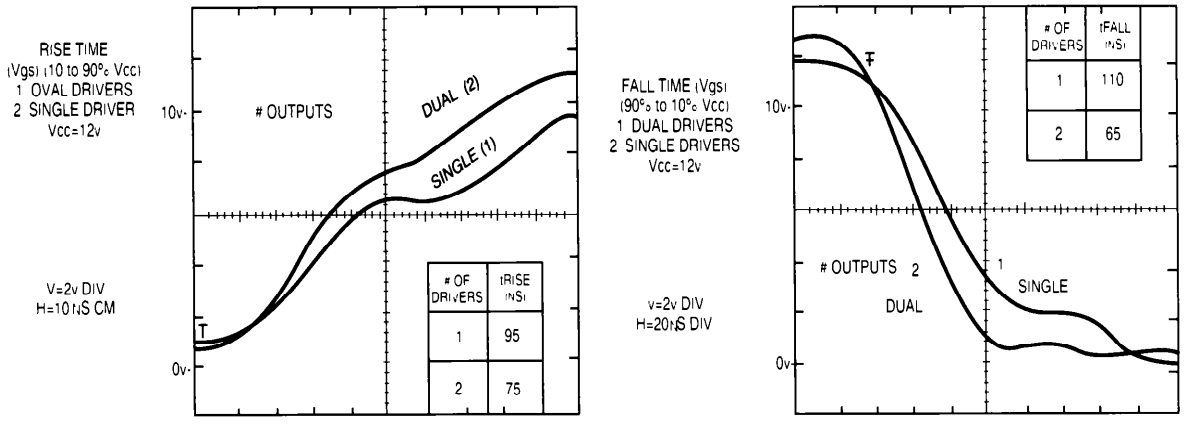


Figure 17

AVERAGE DRIVER CURRENTS DURING TURN-ON & TURN-OFF INTERVAL

EQUATIONS: $Q = CV$; $Q = IT$; $i_{AVG} = \frac{C.V}{T}$

During the transitions between 0 & 10V over Tr & Tf intervals

SINGLE OUTPUT

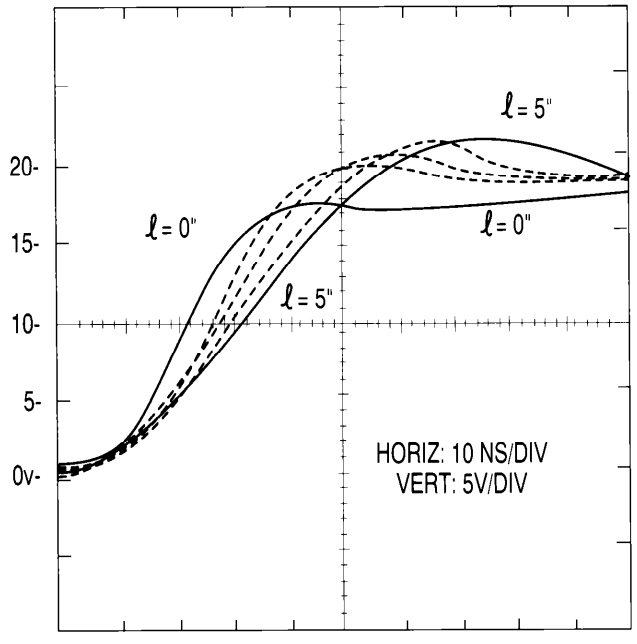
LOAD	RISE	FALL
C = 2.2NF	0.49A	0.67A
C=10NF	1.43A	1.43A
IRFP460	1.26A	1.10A

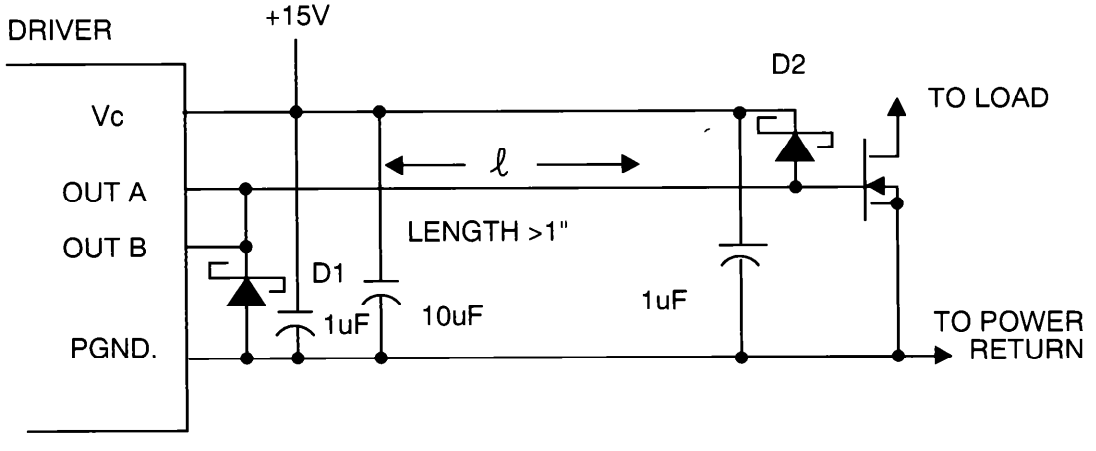
DUAL OUTPUTS

LOAD	RISE	FALL
C = 2.2NF	0.63A	0.88A
C = 10NF	2.0A	2.22A
IRFP460	1.6A	1.85A

While directly connecting the FET gate to the output of the driver is straightforward for testing purposes it does not represent the "real" application which may include several inches or wire or printed circuit board traces, Here, wiring inductance will sharply degrade the transitions and cause substantial overshoot by ringing with the gate capacitance. Extreme examples of this can cause the gate-to-source voltage to overshoot beyond the specified maximum ratings.

Additionally, negative transitions (below ground) at the deriver output can raise havoc with the internal circuitry, leading to undesirable performance. While this is more of a concern with PWMs, (which use low level analog input signals) it will also detract from the drivers peak performance. Both of these conditions can easily be avoided by Schottky clamping the circuit to the auxiliary supply rails.





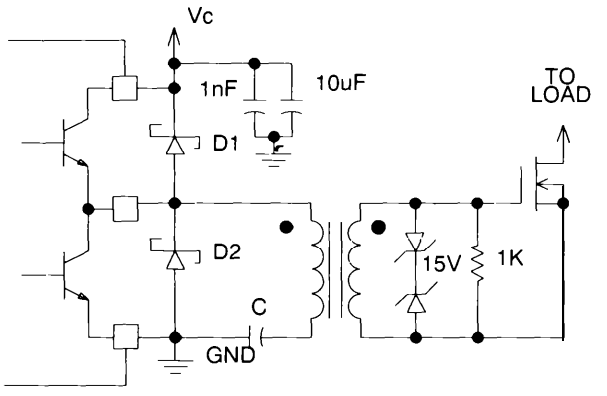
D1 ,D2 : UC3611 OR IN5820

Figure 19

ISOLATED GATE DRIVE

In certain applications, the PWM is referenced to the load or secondary side of the power supply and the gate drive is transformer coupled across the isolation boundary to the power FETs. While this technique may work adequately at low switching frequencies, any series circuit inductance, as shown, will significantly degrade switching speeds and performance as the frequency is increased. An improved version of this circuit locates the drivers on the primary side, as close as possible to the FETs, and transformer couples only the low power input signals. Although somewhat more elaborate, significant improvements in turn-on and turn-off switching times are obtained and the FET switching losses are minimized.

TRANSFORMER COUPLED MOSFET DRIVE CIRCUIT



D1.D2:UC3611 SCHOTTKY DIODE ARRAY

Figure 20

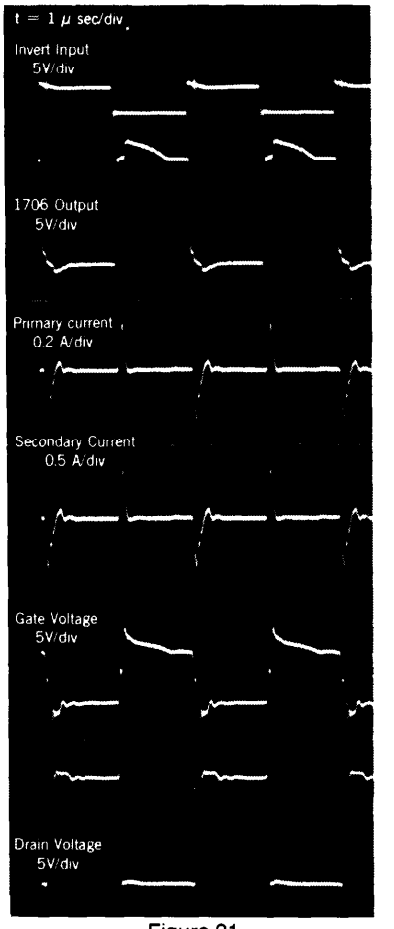


Figure 21

IMPROVED XFMR COUPLED DRIVE CIRCUIT

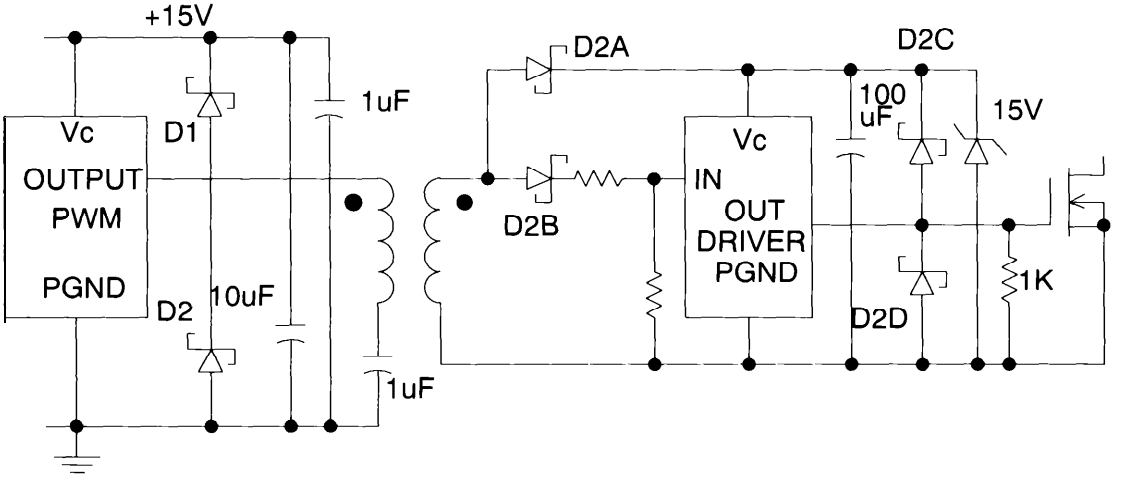


Figure 22

PUSH-PULL TRANSFORMER COUPLING

The totem-pole outputs of the UC3706 can easily be configured for implementing the balanced transformer drive as shown in figure24. Outputs A and B are alternating now as the internal flip-flop is active and the output frequency is halved. Note that when one UC3706 output goes high, the other is held low during the dead time between output pulses. With balanced operation, no coupling capacitor on the primary is necessary since there is no net DC in the primary. Schottky clamp diodes on the primary side and back-to-back zeners on the secondaries are necessary to minimize the overshoot causes by the ringing of the gate capacitance with circuit inductances. Waveforms of all significant points within this circuit are shown.

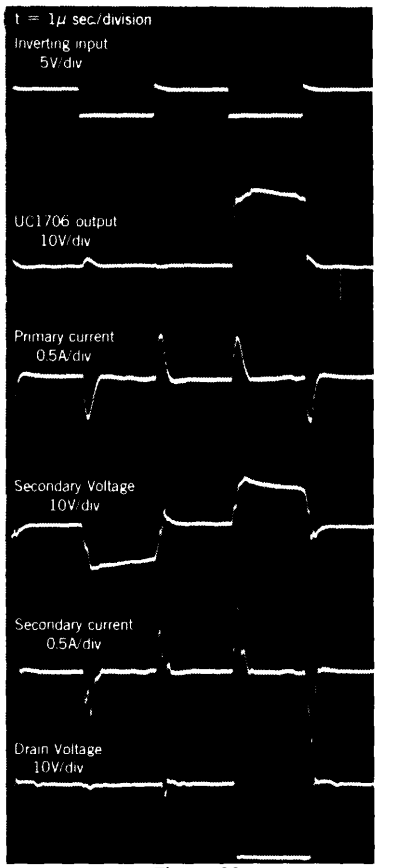


Figure 23

UC 3706 CONVERTS SINGLE OUTPUT PWMS TO HIGH CURRENT PUSH-PULL CONFIGURATION

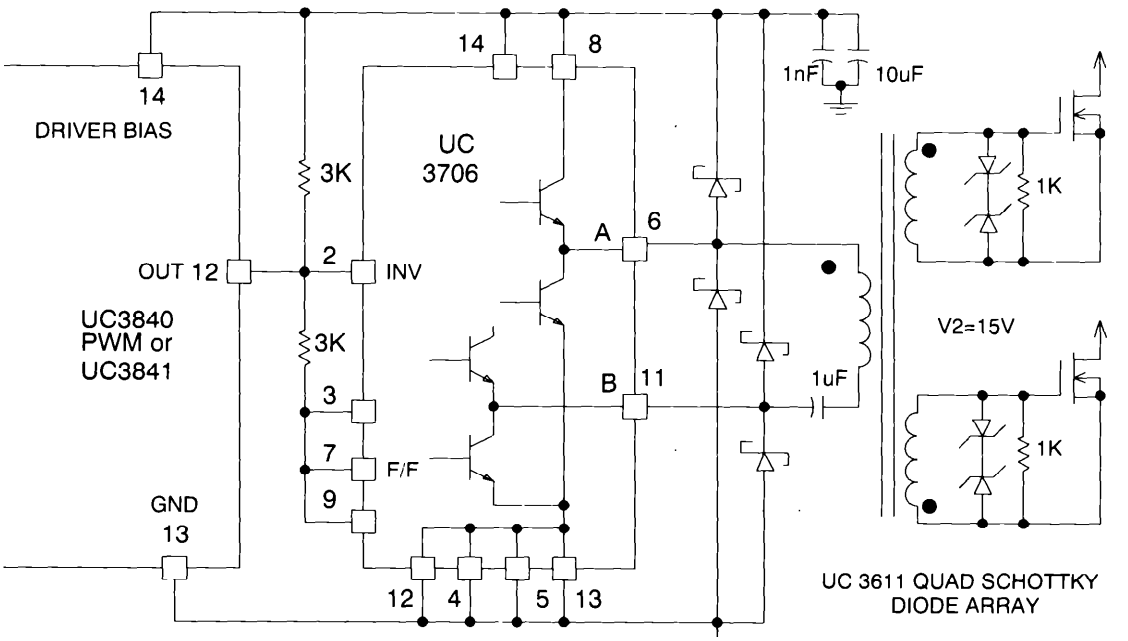


Figure 24

SUPPLYING POWER TO THE DRIVERS

From the block diagrams of figures 6 thru 8, note that the UC3705 UC3706 and UC3707 have two supply terminals, Vin and Vc. These pins can be driven from the same or different voltages and either can range from 5 to 40 volts. Vin drives both the input logic and the current sources providing the pull-up for the outputs. Therefore, Vin can also be used to activate the outputs and no current is drawn from Vc when Vin is low. This is useful in off-line applications where its desirable for the control circuit to have a low start-up current. Several PWM controllers, like the UC1840, UC1841 and the UC1851 feature a Driver Bias output which goes high once the undervoltage lockout threshold is crossed, thus supplying bias to the driver. Adaptations of this technique can be made to work with a variety of other PWMs and control circuits.

USING "SPLIT" SUPPLIES

Many applications utilize a negative voltage rail in the drive circuit to guarantee complete turn-off of power MOSFETs, especially those with low gate threshold voltages, typical of "logic level" input devices. This is easy to implement with any of the UC3705 thru UC3709 drivers by offsetting the input signals with a zener diode equal in voltage to the negative supply, Vee. Although referenced at the driver IC to the Vee rail, these inputs are offset by an equal amount to the PWM controller, simulating a ground referenced input. This technique also offers moderate improvements in FET switching speeds at the penalty of slightly increased effective delay times from the driver inputs. The end results are listed below, which may be beneficial in applications where a tailored gate drive is required to alter the MOSFET switching characteristics.

POWER MOSFET DRIVE CIRCUIT
USING NEGATIVE BIAS VOLTOGE AND LEVEL SHIFTING
TO GROUND REFERENCED PWMS

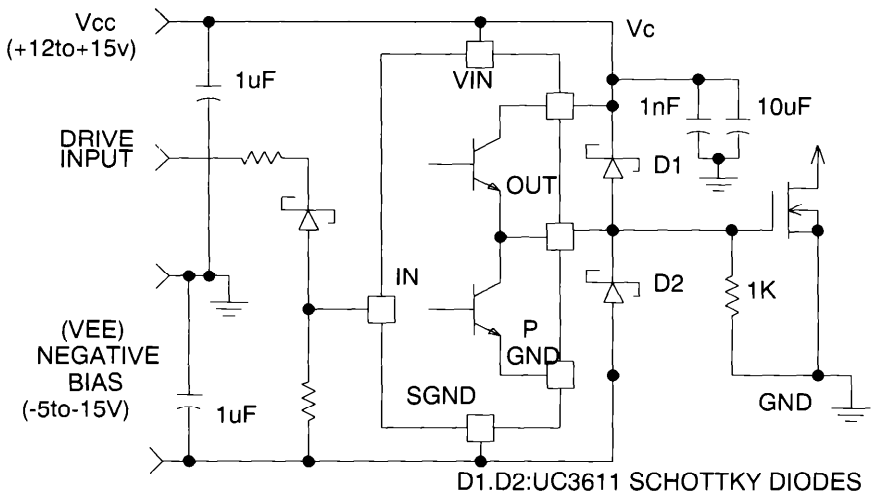


Figure 25

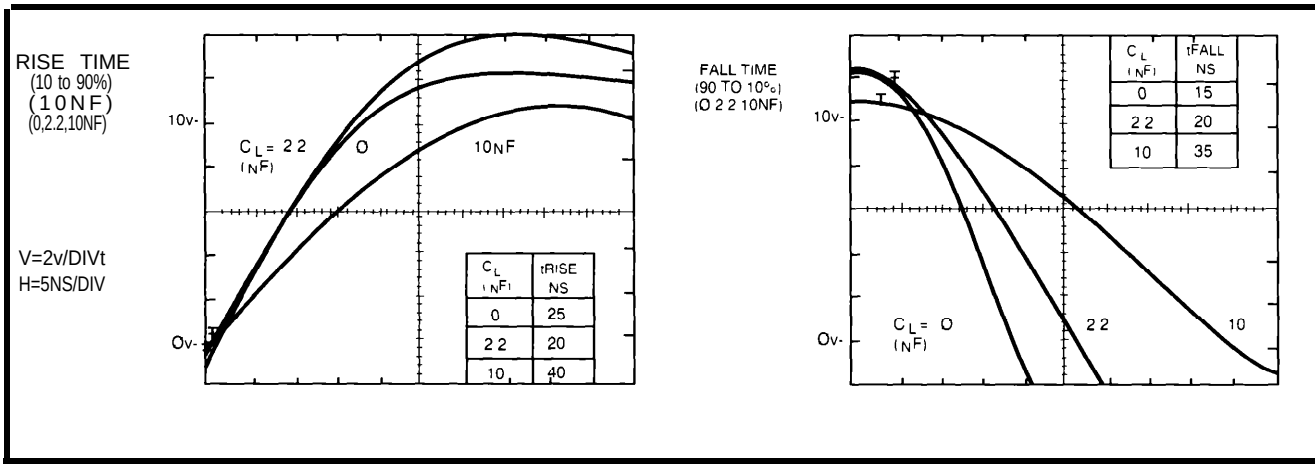


Figure 26

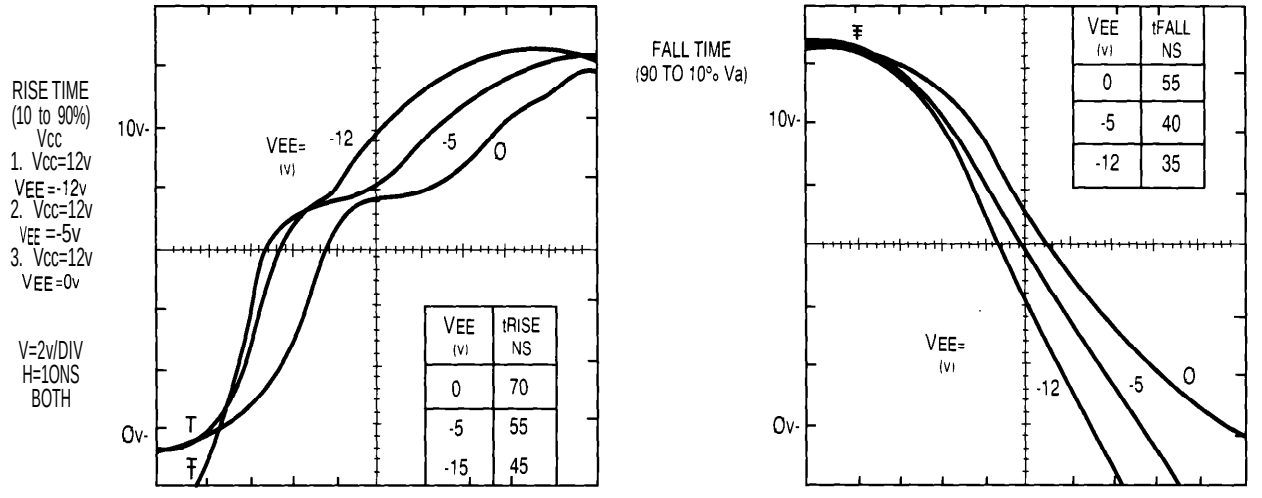


Figure 27

VEE (V)	td Rise to '0" V (NS)	T Rise 0-10V (NS)	Td Fall to begin (NS)	T Fall 10-0V (NS)I	T Delay total (NS)	Tr & Tf total (NS)	T Total tr+tf+trd (NS)
0	56	50	50	45	106	95	201
-5	70	42	50	33	120	75	195
-10	86	34	50	29	136	63	199
-12	93	32	50	28	143	60	203
-15	100	30	50	27	150	57	207

VEE (V)	Delay trd+tfd (NS)	Transition Times tr+tf (NS)
0	Minimum (106NS)	Maximum (95NS)
-15V	Maximum (143NS)	Minimum (60NS)

VEE (V)	Rise	Fall
0	2.4A	2.67A
-5	2.86A	3.64A
-10	3.53A	4.14A
-15	4.0A	4.4A

SUMMARY

This paper has presented an understanding of the dynamics of high speed power MOSFET switching in an attempt to define the optimum gate drive requirements to meet specific applications. The need for high peak gate currents with controlled rise times has led to the development of several integrated circuits aimed towards achieving these goals. The UC3705, UC3706, UC3707 and UC3709 drivers provide high speed response, 1.5 amps of peak current per output and ease the implementing of either direct or transformer coupled drive to a broad range of power MOSFETs. With these new devices, one more specialized function has been developed to further aid the power supply designer simplify his tasks and enhance power MOSFET switching characteristics.

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